IV / SEM / ELECT / 2018(W) **[24/05/2018, EX-REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 70

Time: 3 Hours

Answer any **FIVE** Questions

The figures in the right-hand margin indicate marks

1. **(a)** Convert binary number $(110101.011)_2$ to decimal number. **[2]**

(b) Design 3 : 8 decoder with neat circuit diagram. **[5]**

(c) Which gates are referred to as universal gates and why? How other gates can be implemented by using NAND gates only? **[7]**

2. **(a)** Perform Excess-3 Subtraction of 97 – 72. **[2]**

(b) Simplify the Boolean expression Y (A, B, C) = $A[B + C(\overline{AB + AC})]$. Also draw the logic circuit using NAND gates only. **[5]**

(c) Explain the working of Full adder. Draw its logic circuit and truth table. **[7]**

3. **(a)** Define modulus of a counter. **[2]**

(b) Explain the operation of **7** segments display. **[5]**

(c) Simplify the following expression using the k-map for 4 variable.
F(A,B,C,D) = $\sum m$ (0, 2, 4, 5, 6, 7, 8, 10, 13, 15) & implement this circuit by NAND gate. **[7**

4. **(a)** What is an encoder and where it is used? **[2]**

(b) Differentiate between asynchronous and synchronous counters. **[5]**

(c) With neat diagram explain the operation of a clocked SR Flip flop with a functional table. **[7]**

5. **(a)** State associative and distributive law. **[2]**

(b) With a neat diagram explain the operation of PIPO and PISO shift register. **[5]**

(c) Explain the working of MOD – 10 binary counter with neat diagram. **[7]**

6. **(a)** Write the truth table of a NAND gat with symbol. **[2]**

(b) With a neat circuit diagram explain the function of **1: 8** DE-MUX. **[5]**

(c) Explain R-2R ladder type DAC with a neat diagram. **[7]**

7. **(a)** Which code is known as self correcting code and why? **[2]**

(b) Differentiate between combinational and sequential logic circuit. **[5]**

(c) Draw the logic diagram of Master-Slave JK Flip-Flop. Explain it with a functional table. **[7]**

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Collected By:-

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IV/SEM/ELECT/2017(W) **[17/05/2018, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 70

Time: 3 Hours

Answer any **FIVE** Questions

The figures in the right-hand margin indicate marks

1. **(a)** Convert $(101011110.1011)_2$ to octal and hexadecimal numbers. **[2]**
(b) Discus 1: 4 De-multiplexer with circuit, truth table and implementation by gates. **[5]**
(c) Which gates are referred to as universal gates and why? How other gates can be implemented by using one of these gates? **[7]**

2. **(a)** Define racing condition. How it can be avoided. **[2]**
(b) Design an 8 : 3 encoder with neat circuit diagram. **[5]**
(c) Show the logic diagram of clocked JK-Flip Flop. Explain it's working with a functional table with a neat circuit diagram. **[7]**

3. **(a)** State De-Morgan's theorem. **[2]**
(b) Simplify and minimize the 4-variable logic expression F (A, B, C, D) = $\sum$m (1, 3, 7, 11, 15) + $\sum$d (0, 2, 5) by using k-map and implement its circuit by NAND gates only. **[5]**
(c) Draw the logic circuit of full subtractor. Give its logic expression and truth table. Implement the logic circuit with any one of universal gates. **[7]**

4. **(a)** Define the term fan in, fan out and propagation delay. **[2]**
(b) Explain the working of SISO, PISO shift register with the help of suitable logic diagram. **[5]**
(c) Explain the working of a mod - 8 binary counter with neat diagram. **[7]**

5. **(a)** Find 2's complement substraction of 10110-11010. **[2]**
(b) Simplify the Boolean expression Y = AB + A (B+C) +B (B+C).
And draw the logic circuit for the simplified function. **[5]**
(c) Design a magnitude comparator circuit. Whose outputs are A > B, A = B, A < B.
Where A and B are 2 bit binary numbers. **[7]**

6. **(a)** Distinguish between combinational and sequential logic circuit. **[2]**
(b) Explain weighted and non-weighted binary codes. **[5]**
(c) Define SOP & POS term. Obtain canonical SOP & POS from the function $Y = A+B\bar{C}$. **[7]**

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7. **(a)** Write the truth table of a Exclusive NOR gate. **[2]**
(b) Explain the operation of seven segments display. **[5]**
(c) Draw the diagram of D-Flip flop. Explain its working with functional table. **[7]**

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IV/SEM/ELECT/2017(W) **[28/12/2017, BACK]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 70

Time: 3 Hours

Answer any **FIVE** Questions

The figures in the right-hand margin indicate marks

8. (a) Find the 1's complement and 2's complement of the binary 10110100. **[2]**

(b) With a neat circuit diagram explain the function of 1: 4 Demultiplexer circuits. **[5]**

(c) Which gates are referred to as universal gates and why? How other gates can be implemented by using NOR gates only? **[7]**

9. (a) Convert the decimal number $(95)_{10}$ into its equivalent BCD and Excess-3 Code. **[2]**

(b) Explain the working of Half Adder. Draw its circuit using any one of Universal Gate. **[5]**

(c) Obtain the minimal expression using k-map and draw the logic diagram using NAND gates Only. $F(P, Q, R, S) = \sum m(0, 1, 2, 7, 9, 12, 13) + \sum d(3, 5, 8, 10)$ **[7]**

10. (a) What is max term and min term? **[2]**

(b) With neat logic diagram explain the operation of seven segment display. **[5]**

(c) Design a magnitude comparator circuit. Whose outputs are A > B, A = B, A < B. Where A and B are 2 bit binary numbers. **[7]**

11. (a) Define fan in and fan out. **[2]**

(b) Design a mod -5 synchronous counter with neat circuit diagram. **[5]**

(c) With neat logic diagram explain the working of clocked JK-Flip Flop. Convert this flip flop into its equivalent D-flip flop and T-Flip Flop. **[7]**

12. (a) What is Racing and how it can be avoided? **[2]**

(b) Differentiate between combinational and sequential logic circuit. **[5]**

(c) Explain briefly about SISO, SIPO, PISO and PIPO Shift Registers. **[7]**

13. (a) Draw the block diagram of Full adder using two half adder and one OR gates. **[2]**

(b) With neat sketch explain the working of Decimal to BCD Encoder. **[5]**

(c) Design and explain the working of a 4 bit Ripple counter with neat logic diagram, truth table and timing diagram. **[7]**

14. (a) What is modulus of a counter? **[2]**

(b) Design and explain the working of SR Flip flop using NAND gates with functional table. **[5]**

(c) Explain the working of R-2R Ladder network type D/A converter with neat diagrams. **[7]**

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IV/SEM/ELECT/2017(S) **[APR-2017, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 70

Time: 3 Hours

Answer any **FIVE** Questions

The figures in the right-hand margin indicate marks

1. (a) Which code is known as self correcting code and why? [2]
(b) With a neat circuit diagram explain the function of 1 : 4 Demultiplexer. [5]
(c) Design a 2bit Magnitude Comparator circuit whose outputs are P > Q, P < Q and P = Q Where P and Q are 2 bit nos. [7]

2. (a) Why multiplexers are referred to as data selector? [2]
(b) Show the diagram of a clocked SR Flip-Flop. Explain its working with a functional table. [5]
(c) Simplify and minimize the 4 variable logic express $F(P, Q, R, S) = \sum (0, 2, 4, 6, 8, 12, 15) + d (1, 3, 5, 7)$ by using K-map and implement this circuit by using NAND gate. [7]

3. (a) Define Racing Condition. How it can be avoided. [2]
(b) Design a 4 : 2 Encoder circuit with a neat circuit diagram. [5]
(c) Discuss the operation of an Asynchronous counter with its timing diagram. [7]

4. (a) State de Morgan’s Theorem. [2]
(b) Explain the working of SIPO and PIPO register with the help of a suitable logic diagram. [5]
(c) Which gates are referred to as universal gates and why? How other gates can be Implemented by using any one of the universal gates? [7]

5. (a) Define modulus of a counter. [2]
(b) Differentiate between combinational and sequential logic circuit. [5]
(c) With a suitable logic diagram design a Decade Counter. Write its functional table too. [7]

6. (a) Why Demultiplexers are referred to as data distributors? [2]
(b) Explain the operation of Full Subtractor. [5]
(c) Draw the logic diagram of Master-Slave JK Flip-Flop. Explain it with a functional table. [7]

7. (a) Define Fan In and Fan Out. [2]
(b) Simplify the Boolean expression, $y = \overline{(x\,\bar{y}\,z)(x\,\bar{y}) + y\,z}$ and draw the logic circuit using NAND gates only. [5]
(c) With a neat diagram explain the function of 4 : 1 Mux and 8 : 3 Encoder. [7]

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IV/SEM/ELECT/2016(S) **[APR-2016, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 70

Time: 3 Hours

Answer any **FIVE** Questions

The figures in the right-hand margin indicate marks

1. **(a)** Define Racing Condition. [2]

(b) Which gates are referred to as Universal Gates and Why? How other gates can be realized Using NAND Gates only. [5]

(c) With neat circuit diagram explain the function of 1:4 De-Mux and 4:1 Mux. [7]

2. **(a)** Convert the decimal no. $(1000)_{10}$ into Binary. [2]

(b) Design a 4:2 Encoder with neat circuit diagram. [5]

(c) With neat sketch explain the working of PIPO and SIPO Shift Register. [7]

3. **(a)** Which code is known as self correcting code and why? [2]

(b) A 7 bit hamming code coming out of transmission line is 0010100. If there any error? If Yes, in which data bit and what was the bit data actually transmitted. [5]

(c) Draw the circuit diagram of clocked SR Flip-Flop. Explain it with a functional table. [7]

4. **(a)** Convert (10110101) from binary to gray code. [2]

(b) Distinguish between combinational and sequential logic circuit. [5]

(c) Design a 2 bit magnitude comparator circuit whose outputs are P > Q, P = Q and P < Q, where P and Q are each two bit numbers. [7]

5. **(a)** Perform 2's complement subtraction of 1000011 – 1010111. [2]

(b) Explain the operation of seven segment display. [5]

(c) Sketch logic diagram of clock JK flip – flop. Explain its working with a functional table. [7]

6. **(a)** Define the term Fan out and Resolution. [2]

(b) Describe the operation of full subtractor with the help of truth table and circuit diagram. [5]

(c) Explain the working of 4 bit ripple counter with truth table and timing diagram. [7]

7. **(a)** What is the difference between weighted and non-weighted binary code. [2]

(b) Simplify the Boolen expression:

$a\left[b + c\left(\overline{ab + ac}\right)\right]$. Also draw the logic circuit using NAND gates only. [5]

(c) Simplify the given expression using Kamaugh's Map and draw the logic circuit. Using NAND gate only. $F(a, b, c, d) = \sum m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$ [7]

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IV/SEM/ELECT/2015(S) **[APR-2015, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 70

Time: 3 Hours

Answer any **FIVE** Questions

The figures in the right-hand margin indicate marks

1. **(a)** Convert the binary number $(10110111\ .\ 1101)_2$ to decimal equivalent. [2]

(b) What are the difference between 1's complement and 2's complement? Subtract $(39)_{10}$ and $(25)_{10}$ using 2's complement method. [5]

(c) Explain ASCII code & its application & distinguish between weight and non-weight code. [7]

2. **(a)** What are the application of Gray code? [2]

(b) Draw the symbol, truth table and expression for X – OR and AND gates. [5]

(c) What is universal gate? Explain with examples and realize other gate. [7]

3. **(a)** Define De Morgan's law. [2]

(b) Simplify the expression $Y = \overline{(AB + \bar{C})(\overline{A + B} + C)}$ [5]

(c) Define SOP and POS term. Obtain the canonical SOP form of the function

$Y(A, B, C) = A + \overline{BC}$ and draw the truth table. [7]

4. **(a)** What is parity bit? [2]

(b) Simplify the following expression using the K-map for four variables.

$Y(A, B, C, D) = \sum(1,5,10,11,12,13,15) + d(14,9)$ and implement using AOI gates. [5]

(c) Design a Full adder circuit and implement using NAND gates. [7]

5. **(a)** What are the different between CLC and SLC circuits (any two)? [2]

(b) Explain the working of 2 bit magnitude comparator with logic expression and gate level circuits. [5]

(c) Discuss (1.4) Demultiplexer with logic circuit, truth table and implementation by gates. [7]

6. **(a)** Define fan – in and fan – out. [2]

(b) Define flip-flop and explain clock JK flip-flop using NAND gates only. [5]

(c) Explain the working of 4 bit ripple counter with truth table and timing diagram. [7]

7. **(a)** What is racing condition and how it is avoided? [2]

(b) Explain the working of different types of shift registers. [5]

(c) Explain R – 2R ladder type DAC with a neat diagram. [7]

8. **(a)** Define Resolution and conversation time. [2]

(b) Explain Ramp type ADC with neat circuit diagram. [5]

(c) Explain LED driver Using IC 7447 decoder. [7]

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Collected By:-

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IV/SEM/ELECT/2014(S) **[APR-2014, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 80

Time: 3 Hours

Answer any **FIVE** Questions

The figures in the right-hand margin indicate marks

1. **(a)** State De Morgan's Theorem. [2]

(b) Design a 2 bit magnitude comparator circuit whose outputs are A > B, A = B, A < B, Where A and B are 2 bit numbers. [6]

(c) Define the term offset voltage of D/A converter. Explain the working of weighted resistor type DAC converter with a neat block diagram. [8]

2. **(a)** Find the 2's complement subtraction of 100011 – 1010111. [2]

(b) Which code is known as self correction code and why? A 7 bit hamming code coming out of transmission line is 0010100. Is there any error? If yes, in which data bit and what was the 4 bit data actually transmitted? [6]

(c) Simplify the expression using K-Map

$F(A, B, C, D) = \sum m(4, 7, 12, 15) + d(0, 1, 2, 3, 8, 9, 10, 11)$ & implement it with NAND gate. [8]

3. **(a)** Define Modulus of a counter? [2]

(b) Differentiate between Asynchronous and Synchronous counters? [6]

(c) Draw and write down the function table for the conversion of [8]

(i) SR to JK FF (ii) T to JK FF (iii) SR to D FF (iv) JK to T FF

4. **(a)** Write down the truth table of a 2input Exclusive OR gate? [2]

(b) Show logic diagram of a clocked JK flip-flop. Explain its working with a functional table? [6]

(c) Which gates are referred to as universal gates and why? How other gates can be implemented by using universal gates. [8]

5. **(a)** What do you mean by Fan In, Fan out and propagation delay? [2]

(b) Explain with sketch the working of a 2 input TTL NAND gate? [6]

(c) Draw the logic circuit of full subtractor. Give its logic expression and truth table. Implement the logic circuit with any one of universal gates? [8]

6. **(a)** What is an encoder and where it is used? [2]

(b) With a neat diagram explain the operation of PISO Register? [5]

(c) Design a synchronous 4 bit up down counter using D flip-flops? [7]

7. **(a)** What is racing condition? [2]

(b) Explain the operation of seven segment display and LED? [5]

(c) Design a combinational logic circuit converting 4 bit binary to decimal decoder circuit. [7]

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Collected By:-

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IV/SEM/ELECT/2013(S) **[APR-2013, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 80

Time: 3 Hours

Answer any **FIVE** Questions including Q. nos 1 & 2

The figures in the right-hand margin indicate marks

1. Answer **ALL** question: [2x10]

(a) What is the base or radix of a number system?

(b) Convert $FADE_{16}$ to Binary and Octal.

(c) Convert 7743_g to Binary and Hexadecimal.

(d) Draw the IC pin configuration of NOR gate and IC number.

(e) What is the basic difference between combinational and sequential logic circuit.

(f) What is parity of a binary number?

(g) What are the floating inputs and why they are not allowed?

(h) Define FANIN and FAN out.

(i) Name different IC families and which is fastest family.

(j) What is the difference between RAM and ROM?

2. Answer any **FIVE** question: [5x6]

(a) State and prove Demorgan's theorem. Explain with relevant diagrams, Boolean expressions and functional tables.

(b) What are all the Universal logic gates? Why are they called so? Explain with relevant logic diagrams, Boolean expressions.

(c) Explain the working of a full adder circuit.

(d) Explain the working of a clocked RS flip flop using NAND gates. Why the set and reset inputs are known as asynchronous input signals?

(e) Explain the working of 4 bit SISO register with a neat diagram and timing diagram.

(f) Explain the working of a 4 bit binary asynchronous counter with circuit and timing diagrams.

(g) Explain the terms RAM, ROM, PROM, EPROM and EEPROM.

(h) How the defence application ISs are different from the ICs used in common applications.

3. Explain the working of a 4 bit binary adder subtracter circuit, with neat circuit. [10]

4. Explain the working of a 16:1 multiplexer. [10]

5. Simplify $f(A, B, C, D) = \sum m(0, 1, 2, 5, 6, 8)$ & d(3, 4, 7, 14) using map & draw logic circuit. [10]

6. Explain the working of a synchronous type. Decade counter with neat sketch. [10]

7. Explain the working of a successive approximation type A/D converter. [10]

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IV/SEM/ELECT/2012(S) **[APR-2012, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 80

Time: 3 Hours

Answer any **FIVE** Questions including Q. nos 1 & 2

The figures in the right-hand margin indicate marks

1. Answer **ALL** question: [2x10]

(a) What do you mean by radix of a number system?

(b) Why complementary numbers are used?

(c) State De Morgan's Theorem.

(d) Draw the output waveform of the given logic circuit.

(e) What is the meaning of Min. term and Max. term?

(f) Define demultiplexure and its use.

(g) What is flip-flop and where it is used?

(h) Explain the term 'Fan-in and Fan-out'.

(i) What is the percentage resolution of a 8-bit DAC?

(j) Draw the AOI logic circuit of $Y = \overline{A}.B + \overline{C}.A$.

2. Answer the following in brief (any five): [5x6]

(a) Which gates are called universal gates and how other gates can be realized?

(b) Explain the working of a clocked RS flip-flop using NAND logic circuit.

(c) Simplify Boolean expression $X = \overline{PQ + PR} + \overline{PQ}.R$ & draw logic circuit using NOR gate only.

(d) Distinguish between combinational logic and sequential logic.

(e) Design a 4:1 multiplexer with neat circuit diagram.

(f) What is the necessity of digital code? Differentiate between weighted code and non-weighted code. How Gray code is used to convert to binary?

(g) Define a half adder. How a full adder can be constructed using half adder? Draw the logic circuit and truth table of full adder.

(h) Explain the operation of seven segment display.

(i) With neat circuit diagram, explain the working of 4-bit ripple counter.

3. Simplify the minimal minterm expression of $f(W, X, Y, Z) = \sum m(0, 1, 2, 5, 6, 8) + d(3, 4, 7, 14)$ using Karnaugh map & draw logic circuit using NAND gate only.

4. Explain the working of JK flip-flop and draw its truth table. How JK flip-flop can be constructed into (i) T-flip-flop, (ii) D-flip-flop.

5. Explain working of a Mod-10 binary counter with neat diagram & show its timing diagram. [10]

6. Explain with a sketch the successive approximation A/D converter. [10]

7. Write short notes on any two of the following: [5x2]

(a) Explain the working of SIPO shift register.

(b) One-bit comparator circuit.

(c) Racing condition and how it can be avoided.

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IV/SEM/ELECT/2011(S) **[APR-2011, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 80

Time: 3 Hours

Answer any **FIVE** Questions including Q. nos 1 & 2

The figures in the right-hand margin indicate marks

1. Answer **ALL** question: [2x10]

(a) What is the base of a number system?

(b) Convert $(111101000.0111)_2$ to octal and hexadecimal numbers.

(c) Find the two's complement of a number $(1000000)_2$.

(d) What is donot care condition?

(e) What is parity and how it is used?

(f) What do you mean by latching?

(g) Define modulus of a counter.

(h) Explain the meaning of 'Fan-in' and 'Fan-out' with reference to logic families.

(i) What is Demultiplexer?

(j) What will be the resolution of 16 bits D/A converter?

2. Answer any six: [2x10]

(a) What is Universal gate and how the other gates can be implemented by using any one of the Universal gate?

(b) With neat circuit diagram explain the function of 1:4 Demultiplexer circuit.

(c) Show the logic diagram of a clocked RS flip-flop based on NAND gates. Explain its working with a functional table.

(d) Explain the basic operation of a shift register with neat diagram.

(e) What is self correcting code? Explain the format for self correcting code.

(f) Differentiate between combinational logic and sequential logic.

(g) Explain the working of a Ladder Network type D/A converter with diagram.

(h) Simplify the Boolean expression $F = XY + XYZ + XY\bar{Z} + \bar{X}YZ$ using Boolean algebra and draw the logic circuit.

3. Simplify the minimal SOP and POS expressions $F(A, B, C, D) = \sum(3,4,6,7,11,12,13,14)$ [10]

4. Design a 2-bit digital comparator circuit for comparing two-2bit numbers A and B. [10]

5. Explain the working of 4-bit ripple counter with truth table and timing diagram. [10]

6. What is Racing? How it is eliminated in M/S JK flip-flop? Explain with suitable diagram. How the JK flip-flop is converted into 'D' and 'T' type flip-flop?

7. Write short notes on any two: [5+5]

(a) Seven segment display

(b) Compare between LED and LCD

(c) Full subtractor.

--- ALL THE BEST --- ALL THE BEST ---

IV/SEM/ELECT/2010(S) **[APR-2010, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 80

Time: 3 Hours

Answer any **FIVE** Questions including Q. nos 1 & 2

The figures in the right-hand margin indicate marks

1. Answer **ALL** question: [2x10]

(a) What do you mean by 'Radix' of a number system?

(b) Write the truth table of a AND gate with symbol.

(c) What is Hollerith code and why it is essential?

(d) Draw the K-map of a maxterm expression fro which is represented as

$$F(A, B, C) = (A + B)(B + C)(C + A)$$

(e) What do you mean by Fan-In and Fan-Out?

(f) Define modulus of a counter and why it is essential.

(g) Define NOR Latch.

(h) Use 2's complement subtract 11101-1101.

2. Answer any six: [2x10]

(a) If two inputs A and B having 10101 and 11100 data are applied to the NAND gate inputs, serially determine the output waveform of NAND gate with truth table.

(b) Minimize the following Boolean function using K-map and implement in any one of the universal gates: $F(A, B, C, D) = \sum m(5,7,8,10,13,15) + \sum d(0,1,2,3)$

(c) Design a decimal decoder circuit using gates.

(d) Explain the operation of TTL – NAND gate with a neat circuit diagram.

(e) Explain briefly operation of BCD seven segment decoder.

(f) What is ripple counter and compare between synchronous and ripple counter?

(g) Design a combinational circuit having three input whose output is equal to 1 if the input variables have more 1's than 0's. the output is 0 otherwise.

3. Given the Boolean algebra function $F = xy + x'y' + y'z$ [10]

(a) Implement it with AND, OR and inverter gates.

(b) Implement it with NAND gate only.

(c) Implement it with NOR gate only.

(d) Give its truth table.

4. Explain working of full subtractor with a neat diagram & implement using universal gates. [10]

5. Define clocked JK flip-flop and explain working of JK flip-flop using NAND-NAND and AND-OR with truth table. [10]

6. What is shift register and what are its classification and explain the operation of serial shift-register with neat circuit diagram? [10]

7. Write the short notes on any two: [5+5]

(a) Error detection and correction code

(b) Multiplier

(c) ECL logic.

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IV/SEM/ELECT/2009(S) **[APR-2009, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 80

Time: 3 Hours

Answer any **FIVE** Questions including Q. nos 1 & 2

The figures in the right-hand margin indicate marks

1. Answer **ALL** question: [2x10]

(a) Subtract 0111_2 from 1010_2.

(b) Multiply 1010_2 by 101_2.

(c) Convert the decimal number 268_{10} into hexadecimal and octal number system.

(d) Draw the truth for NAND gate and construct the same using AND and NOT gate.

(e) What is weight code? Where is it used?

(f) Draw the truth table for D-flip-flop and give the symbol of D-flip-flop.

(g) What are the application of full adder circuit?

(h) A 16 x 8 ROM stores the words in its first two location i.e. R_0 = 1011 1111, R_1 = 0011 1100. Express the store contents in decimal and hexadecimal.

(i) Where shift registers are used?

2. Answer any SIX: [2x10]

(a) Design a half adder circuit and implement using NAND gate only.

(b) Writs the function of a clocked JK flip-flop with truth table and necessary circuit diagram.

(c) What are the different characteristics of Digital logic Families?

(d) Explain briefly working of Seven Segment Decoder with a neat circuit diagram.

(e) Mention the difference between weighted and un-weighted codes with suitable examples. Give application of ASCII code.

(f) State and prove De Morgan's theorems with relevant logic diagrams and Boolean's expressions.

3. Explain working of 4 bit synchronous counter. How it can be converted to a decade counter?[10]

4. **(a)** Draw AND – OR logic circuit for the expression (A + B) (C + D) (E + F) and change this to NOR logic.

(b) Explain briefly DTL logic of NAND gates with a neat circuit diagram.

5. Simplify the expression using K-map F (A, B, C, D) = $\sum(1,5,7,8,9,10,11,14,15)$ and implement using NAND gates only. [10]

6. What are different types of shift registers and explain them with a neat circuit diagram. [10]

---✤----☯----ॐ--- **ALL THE BEST** ---✤---📖----ॐ----📖---✤--- **ALL THE BEST** ---ॐ----☯----✤-----

Collected By:-

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IV/SEM/ELECT/2008(S) **[APR-2008, REG]**

DIGITAL ELECTRONICS

Sub Code – **ETT-421**

Full Marks: 80

Time: 3 Hours

Answer any **FIVE** Questions including Q. nos 1 & 2

The figures in the right-hand margin indicate marks

1. Answer **ALL** question: [2x10]

(a) Multiply $(1001.11)_2$ x $(100.11)_2$.

(b) Convert $(A268.12)_{16}$ to Binary and Decimal.

(c) Draw the diode circuit for AND gate.

(d) Draw the truth-table and symbol for NAND gate.

(e) What is D Latch?

(f) What are the families of ICs that are widely in use? Which is the fastest of them?

(g) What do you mean by modulus of counter?

(h) What is 7-bit code and whether it is weighted or non-weighted?

2. Answer any six: [2x10]

(a) Why NAND and NOR gates are called universal gate? Justify your answer.

(b) Realize EX – OR gate using minimum no of NAND gate & give truth table for EX-OR gate.

(c) State and prove de Morgan's theorem.

(d) Explain the working of a Half Adder using NAND gate only.

(e) Draw a 4-bit ripple counter and explain its working.

(f) What is flip-flop? Explain the working of a clocked JK flip-flop.

(g) An AND gate is followed by a NOT gate. With inputs A and B, obtain the Boolean expression of the output C. Draw its truth table.

3. **(a)** Simplify the following Boolean function is product of sums:

F(A, B, C, D) – S(0, 1, 2, 5, 8, 9, 10) [6]

(b) What is the simplified sum of product form of F?

4. **(a)** Draw the internal circuit configuration of a TTL NAND gate. [5]

(b) Using Boolean algebra, write an expression for output Y of circuit. Hence identify the circuit

5. Explain the working of a decade counter and draw its timing diagram. [10]

6. Write short notes on any two of the following [5 x 2]

(a) Shift register

(b) Full adder circuit

(c) Working of decoder

--- ALL THE BEST --- ALL THE BEST ---

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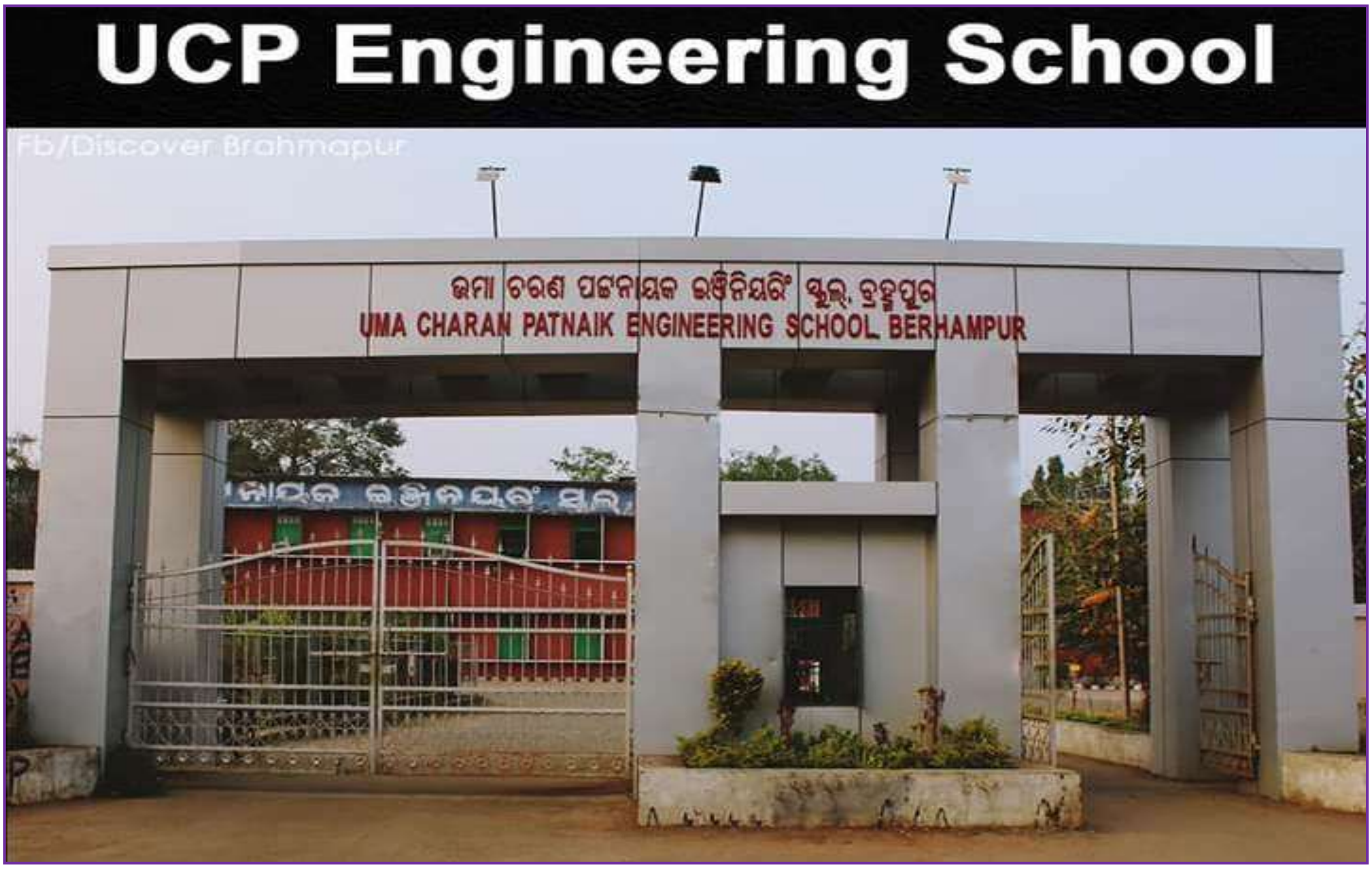
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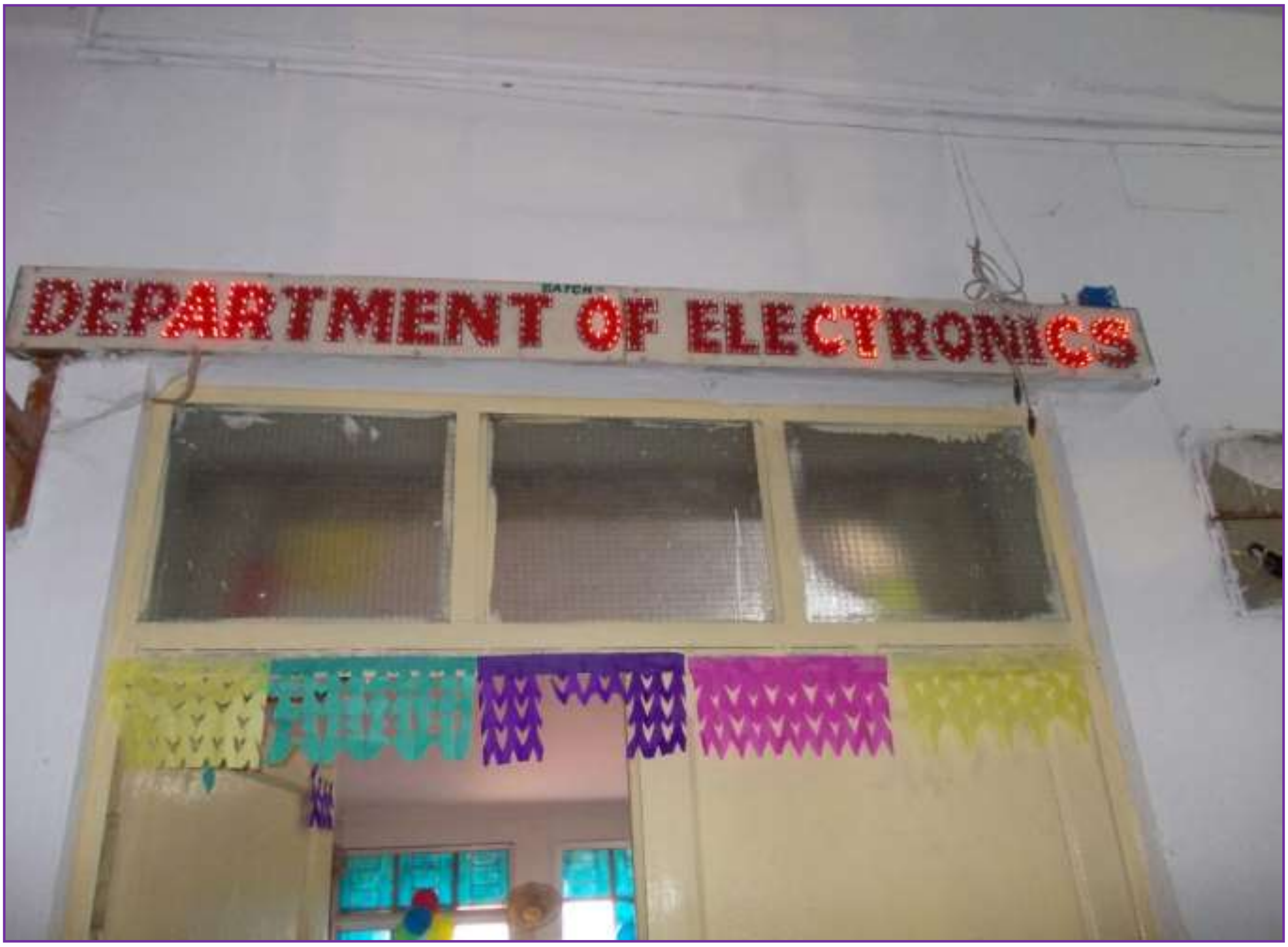
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